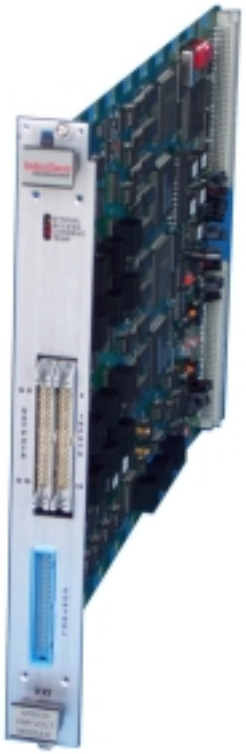
SR5030

Variable Voltage I/O Module For SR5000 Digital Test Subsystem



- 16 Input and 16 Output Pins per Module
- 4 Programmable Input and Output Levels per Module
- 64K Vectors per Channel
- 50 MHz Data Rate
- RAM-Backed and Algorithmic Pattern Generation
- NRZ, RZ, RONE, RTC, and RI Output Data Formats Supported
- 10 Timing Generators per Module
- 100 ps Edge Placement Resolution

Variable Voltage I/O

The SR5030 provides a variable voltage interface to the unit under test (UUT). Up to 20 SR5030 I/O modules can be controlled by the SR5010 Timing/Control Module for a total of 320 I/O pins. The inputs and outputs of the SR5030 can operate over a range of -6 volts to +15 volts. This range is sufficient to cover TTL, CMOS, ECL, and most military and non-standard logic levels. The SR5030 Variable Voltage I/O Module contains 16 stimulus and 16 response channels on a single VXI C-size card.

Seven Distinct I/O Memory Types

The SR5030 I/O Module contains seven separate memory banks, each 64K vectors in depth, for generating stimulus patterns, expected response patterns, and recording UUT response data.

The Stimulus Memories contain the Output, Algorithmic and Tristate patterns, which are used to define the stimulus output to the UUT. The Response Memories contain the Expect, Algorithmic, and Mask patterns, which are used to define the expected response from the UUT.

Record Memory is used to store either the UUT response data or the result of the comparison between the UUT response data and the Expect pattern. It is operated independently in a manner much like a logic analyzer. A sixteen-level state machine and nine system-wide digital comparators are used to control what data is saved in the memory. In addition to the record memory, each input channel is provided with a 16-bit CCITT CRC register for Signature Analysis applications.

Timing and Voltage Control

Each I/O module contains 10 separate timing generators for stimulus and response edge placement. Output pins can select from 4 timing generators to define the leading and trailing edges of each stimulus pin. Groups of eight output pins share an independent set of 4 timing generators for a total of 8 stimulus timing generators per card. Response pins can select from 2 response timing generators to define the sample and compare edges, or the 2 response timing generators can be combined together for window compare with glitch detection.

The output high and low voltages and the input logic threshold voltage are independently user programmable in groups of four channels. The output skew rate is internally controlled according to the output level.

Multiple Data Formats

Stimulus pins may be independently programmed for any of the following formats: Non Return to Zero (NRZ), Return to Zero (RZ), Return to One (RONE), Return to Complement (RC) and Return to Inhibit (RI).

*SR5030 SPECIFICATIONS**

Channels per Module:

Inputs	16
Outputs	16

Memory Types:

Stimulus	Output, Tristate, Algorithmic
Response	Expect, Mask, Algorithmic
Record	

Memory Depth:

65,500 vectors

Output Drivers:

Type	Variable Voltage
Voh	-5.5 V to +15 V, unterminated
Vol	-6.0 V to +14.5 V, unterminated
Output Swing	0.5 V to 21 V p-p, unterminated
Output Current	± 50 mA, maximum
Output Protection	Current and temperature
Abs Max Volt	-7.0 V to +16 V (high Z)
Output Impedance	50 ohms, ± 10%
Voltage Resolution	0.01 volt
Absolute Accuracy	0.1 volt
Slew Rate	1 volt/ns, nominal: internally controlled according to output level

Data Formats:

RZ	Return to Zero
NRZ	Non-Return to Zero
RONE	Return to One
RC	Return to Complement
RI	Return to Inhibit/Tristate

Output Timing:

Clock Pairs	4 total per card (assert/deny) 2 per eight channels
Delay Range	One clock period
Pulse Width	10 ns, min. (high or low)
Resolution	100 ps, non-monotonic 2.0 ns, monotonic
Delay Accuracy	2.0 ns, typ; 3.0 ns, max. (single channel)
Pulse Width	3.0 ns, typ; 5.0 ns, max. Accuracy

Skew:

Same Module	±2 ns typical, ±4 ns maximum
SR5030-SR5030	±3 ns typical, ±5 ns maximum

Input Receivers:

Type	Variable Threshold
Input Thresh. Range	-6 V to +12 V
Vth Resolution	0.01 V
Vth Absolute Accuracy	0.1 V
Input Hysteresis	60 mV p-p, typical
Input Resistance	30k ohms, typical to Vth
Input Termination	Jumper selectable: none, 50 ohms to ground, or 50 ohms to -2.0 V

Input Sample / Compare Modes:

Formats	Edge / window
Range	One period clock cycle
Resolution	100 psec
Accuracy	±1 ns typical; ±2 ns maximum

Input Timing:

Number of Timing Clocks	Two per card (edge mode); one per card (window mode)
Input Delay Range	One clock period
Clock Separation	10.0 ns, minimum
Resolution	100 ps, non-monotonic; 2.0 ns, monotonic

VXI Specifications

Interface Compatibility:

Type	Register-based, servant only (controlled by SR5010)
Revision	1.3 and 1.4
Size	C-size, single slot
Configuration	Static
Memory	2 MB VME A32/D32

Power Requirements:

+5.0 volts	5.0 A	25.0 W
-5.2 volts	2.5 A	13.0 W
+12.0 volts	0.1 A	1.20 W
+24.0 volts	1.6 A	38.4 W
-24.0 volts	0.75 A	18.0 W
-12.0 volts	0.1 A	1.20 W
-2.0 volts	2.0 A	4.00 W

Total Power		100.8 W (max.)

Cooling Requirements:

Per-slot Average	101 W (max.)
Airflow	8 L/sec @ 0.38 mm water pressure for 10°C temperature rise

Environmental Specifications:

Temperature	Storage = -40°C to +75°C Operating = 0°C to +45°C
Humidity	5% to 95% relative, noncondensing

Software Drivers:

National Instruments	LabView
National Instruments	LabWindows/CVI

* Specifications subject to change without notice.

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